embodied in other ways. For example, silicide layers (indicated by bold lines in FIGS. **1** to **5**C) may be formed on surfaces of the n^+-type layers **315**, **316**, **325**, **326**, **338**, **339**, **415**, **416**, **425**, **426**, **438**, **439**, **466**, **516**, **517**, **560**, **538**, **548**, **570** and the p^+-type layers **341**, **342**, **352**, **353**, **368**, **369**, **446**, **448**, **515**, **525**, **526**, **528**, **537**, **547**, **556**, **558**, **644** to reduce the contact resistances. Further, silicide layers (indicated by bold lines in FIGS. **1** to **5**C) may be formed on surfaces of the gate electrodes of the polysilicon films to reduce the resistances of the gate electrodes.

[0087] The BiCDMOS element is merely required to include at least one n-channel double diffusion MOS transistor, at least one CMOS element and at least one bipolar element provided on the common semiconductor substrate, and the passive elements are not necessarily required to be provided on the common semiconductor substrate.

[0088] Further, the n-channel double diffusion MOS transistor according to the present invention is not necessarily required to be incorporated in the semiconductor composite device.

[0089] The impurity ion species, the doses and the acceleration energies are shown by way of example, and may be arbitrarily determined.

[0090] The present application corresponds to Japanese Patent Application No. 2013-012276 filed in the Japan Patent Office on Jan. 25, 2013, and the entire disclosure of the application is incorporated herein by reference.

[0091] While preferred embodiments of the present invention have been described above, it is to be understood that variations and modifications will be apparent to those skilled in the art without departing the scope and spirit of the present invention. The scope of the present invention, therefore, is to be determined solely by the following claims.

What is claimed is:

1. An n-channel double diffusion MOS transistor comprising:

a p-type semiconductor substrate;

a p-type epitaxial layer formed on the p-type semiconductor substrate through epitaxial growth;

an n-type buried layer provided in a boundary between the p-type semiconductor substrate and the p-type epitaxial layer;

a p-type body layer provided in a surface portion of the p-type epitaxial layer;

an n-type source layer provided in the p-type body layer and defining a double diffusion structure together with the p-type body layer;

an n-type drift layer provided in a surface portion of the p-type epitaxial layer in spaced relation from the p-type body layer to define a channel region between the n-type source layer and the n-type drift layer;

an n-type drain layer provided in a surface portion of the p-type epitaxial layer in spaced relation from the channel region and in contact with the n-type drift layer;

a p-type buried layer buried in the p-type epitaxial layer between the n-type drift layer and the n-type buried layer in contact with an upper surface of the n-type buried layer and having a lower impurity concentration than the n-type buried layer;

a gate insulation film provided in a surface of the p-type epitaxial layer on the channel region; and

a gate electrode provided in opposed relation to the channel region with intervention of the gate insulation film.

2. The n-channel double diffusion MOS transistor according to claim **1**, wherein the n-type buried layer continuously extends through a region at least including regions present under the p-type body layer, the channel region, the n-type drift layer, the n-type source layer and the n-type drain layer.

3. The n-channel double diffusion MOS transistor according to claim **1**, wherein the p-type buried layer is provided in a region including regions present under the n-type drift layer and the n-type drain layer.

4. The n-channel double diffusion MOS transistor according to claim **1**, wherein the p-type buried layer is absent from a region present under the p-type body layer.

5. The n-channel double diffusion MOS transistor according to claim **1**, wherein the p-type buried layer is absent from a region present under the channel region.

6. The n-channel double diffusion MOS transistor according to claim **1**, further comprising an insulator buried structure provided between the n-type drain layer and the channel region in the n-type drift layer to extend a current path in the n-type drift layer.

7. The n-channel double diffusion MOS transistor according to claim **1**, further comprising an n-type well provided in contact with the n-type buried layer to surround the p-type body layer, the channel region, the n-type drift layer, the n-type source layer and the n-type drain layer to define an active region.

8. A semiconductor composite device comprising:

an n-channel double diffusion MOS transistor as recited in claim **1**;

a CMOS element provided on the p-type semiconductor substrate; and

a bipolar element provided on the p-type semiconductor substrate.

9. The semiconductor composite device according to claim **8**, further comprising at least one functional element selected from the group consisting of a p-channel DMOS transistor, a p-channel MOS transistor, an n-channel MOS transistor, a resistor element, a capacitor element and a diode element.

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